## AMENDMENTS

### TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### LISTING OF CLAIMS:

1. (previously presented): A constant current bias circuit associated with a linear power amplifier comprising:

an at least one resistor;

a capacitor coupled to the at least one resistor;

a bias voltage input terminal for receipt of a bias voltage connected to the at least one resistor; and

an at least one transistor connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

2. (currently amended): The constant current bias circuit of claim 1, further ~~comprising~~including:

a clamp circuit coupled by an electrical path to the at least one resistor that provides a minimum bias current.

3. (original): The constant current bias circuit of claim 1, wherein the bias current is in a linear relationship with the bias voltage.

4. (currently amended): The constant current bias circuit of claim 1, further ~~comprisingincluding~~:

a circuit having a plurality of components electrically coupled to the at least one resistor in receipt of the bias current.

5. (currently amended): The constant current bias circuit of claim 4, wherein the at least one resistor is in a first material in a substrate and at least one component of the plurality of components is in a second material in the substrate and different from the first material.

6. (original): The constant current bias circuit of claim 5, wherein the first material is Complementary Metal Oxide Semiconductor fabrication material.

7. (original): The constant current bias circuit of claim 6, wherein the second material is Gallium Arsenide Semiconductor fabrication material.

8. (original): The constant current bias circuit of claim 4, wherein the circuit is a single stage amplifier.

9. (original): The constant current bias circuit of claim 4, wherein the circuit is a multi-stage amplifier.

10. (currently amended): The constant current bias circuit of claim 1, further ~~comprising~~including a feedback loop that maintains a quiescent bias for a reference transistor included in the feedback loop equal to a reference current, wherein the reference current is mirrored from the bias current.

11. (currently amended): A constant current bias circuit associated with a linear power amplifier comprising:

an at least one resistor;

a capacitor coupled to the at least one resistor;

means for receiving a bias voltage connected to the at least one resistor; and

an at least one transistor connected to the at least one resistor by an electrical path resulting in a bias current when the bias voltage is present.

12. (currently amended): The constant current bias circuit of claim 11, further ~~comprising~~including [[:]]means for providing a minimum bias current coupled by an electrical path to the at least one resistor.

13. (original): The constant current bias circuit of claim 11, wherein the bias current is in a linear relationship with the bias voltage.

14. (currently amended): The constant current bias circuit of claim 11, further ~~comprising~~including [[:]]a circuit having a plurality of components electrically coupled to the at least one resistor in receipt of the bias current.

15. (currently amended): The constant current bias circuit of claim 14, wherein the at least one resistor is in a first material in a substrate and at least one component of the plurality of components is in a second material in the substrate and different from the first material.

16. (original): The constant current bias circuit of claim 15, wherein the first material is Complementary Metal Oxide Semiconductor fabrication material.

17. (original): The constant current bias circuit of claim 16, wherein the second material is Gallium Arsenide Semiconductor fabrication material.

18. (original): The constant current bias circuit of claim 14, wherein the circuit is a single stage amplifier.

19. (original): The constant current bias circuit of claim 14, wherein the circuit is a multi-stage amplifier.

20. (currently amended): The constant current bias circuit of claim 11, further ~~comprising~~including a means for generating a feedback loop to maintain a quiescent bias for a reference transistor included in the feedback loop equal to a reference current, wherein the reference current is mirrored from the bias current.

21. (currently amended): A method for constant current biasing associated with a linear power amplifier, the method comprising:

receiving an input bias voltage; and

generating a bias current ~~$I_{ref}$~~$I_{bias}$ by at least one resistor connected by an electrical path to at least one transistor being in receipt of the input bias voltage.

22. (currently amended): The method of claim 21, further ~~comprising~~including the step of [[:]]determining if the input bias ~~current~~voltage is ~~above~~below a predetermined threshold.

23. (currently amended): The method of claim 22, further ~~comprising~~including the step of [[:]]activating a clamp circuit to assure the bias current $I_{bias}$ is above a predetermined threshold.

24. (currently amended): The method of claim 21, further ~~comprising~~including the step of [[:]]mirroring the bias current ~~$I_{ref}$~~$I_{bias}$ to a ~~base~~reference current ~~$I_{base}$~~$I_{ref}$ by a predetermined ratio.

25. (currently amended): The method of claim [[21]]24, further ~~comprising~~including the step of [[:]]receiving the ~~bias~~reference current $I_{ref}$ at a transistor in a ~~first~~second material different from a ~~second~~first material, wherein the bias current was generated in the ~~second~~first material.

26. (currently amended): The method of claim 25, wherein the ~~second~~first material is CMOS and shares a substrate with the ~~first~~second material.

27. (currently amended): The method of claim 21, further ~~comprising~~including the step of [[:]]maintaining a feedback loop ~~of~~that provides a quiescent bias for a reference transistor included in the feedback loop equal to [[the]]a reference current $I_{ref}$, wherein the reference current $I_{ref}$ is mirrored from the bias current $I_{bias}$.